

Electromigration in Cu Interconnects

This work is intended for the beginners and the advanced readers. Electromigration in VLSI/ULSI interconnection remains one of the major failure issues in microelectronics and electromigration remains an attractive research area in last few decades. This work attempts to explore the driving force formalism of the electromigration phenomenon. The prime interest of this work is to investigate the physics of failure in submicron (down to 100 nm wide) Cu interconnections including the effect of surrounding materials. A combined driving force model, including the forces from the stress and temperature gradients is presented. In order to develop the combined driving force model, commercial finite element analysis package is used. Plenty of experiments on Cu damascene interconnects are conducted, and extensive failure analyses are performed to investigate the root causes of electromigration failure. Good correlations between the model predictions and experiments are obtained. The future challenges on the study of electromigration are also discussed.

Dr. Arijit Roy

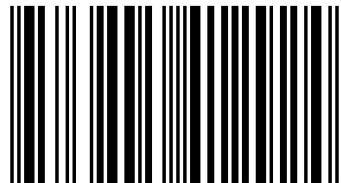
Electromigration in Cu Interconnects

The Driving Force Formalism: Modeling and Experiment



Dr. Arijit Roy

Dr. Arijit Roy has attended many prestigious institutes like IITs, NTU (Singapore) and Infineon Technologies. He has published many research articles and contributed significantly on Electromigration. Presently, he is assistant professor in the department of Electronics at WBSU (India), where he is driving for excellence in teaching and research.



978-3-8454-1292-4

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Academic Publishing